LOGIC DESIGNS USING THE TTμL 9008

by Clive Ghest

INTRODUCTION

The TTμL 9008 is a member of the Fairchild CCSL, compatible current sinking logic family of digital integrated circuits. The high speed and versatility of the element make it an attractive device for high speed digital computers and data acquisition systems. The TTμL 9008 (Fig. 1) consists of three two-input AND gates and one three-input AND gate all feeding into a NOR gate. The NOR gate has the ability to extend the number of connected AND gates to eight. The element has the same high-speed and fan-out as the TTμL NAND gate but with a power consumption approximately the same as that for the equivalent logic function performed in DTμL.

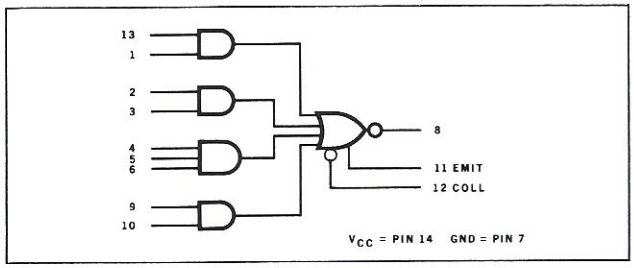

Fig. 1. TTμL 9008.

The element allows the familiar wire-OR function performed in DTμL to be logically produced in TTμL. (See Fig. 2.)

Since the expanding capability allows a total of eight AND gates to connect to the NOR gate, the 9008 can produce the logic equivalent of eight wire-OR'd DTμL NAND gates and the device still maintains full drive capability. This is a substantial improvement over DTμL, where only six NAND gates can be wire-OR'd and this reduces the fan-out to three.

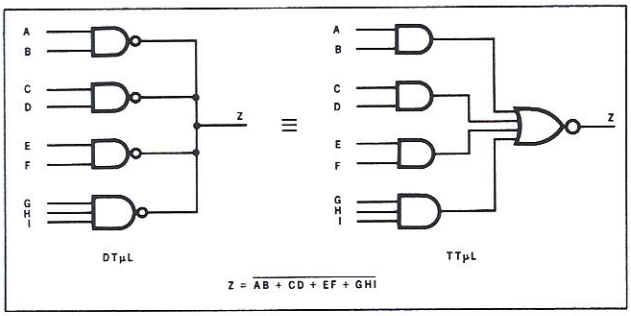

Fig. 2. Comparison of wire "OR" in DTμL and TTμL.

However, the high speed of the 9008 with its associated fast rise and fall times necessitates increased attention paid to packaging, with perhaps additional cost when compared to a design using DTμL elements. The user is advised to consider alternatives offered by the DTμL and LPDTμL groups of circuits in the CCSL family of devices if a low speed system is contemplated.

REGISTER GATING

The 9008 can be used to gate four registers to a single data bus. This number can be increased to eight with the use of the expanding capability to increase the number of connected AND gates. When more than eight registers are required to connect to a single bus, several 9008 elements can feed into a NAND gate, which increases the number of connected registers at the expense of additional logic delay. The extra input provided on one of the AND gates in the 9008 element can conveniently be used as an inhibit input for special purpose logical or arithmetic operations such as a square root computation (Fig. 3).

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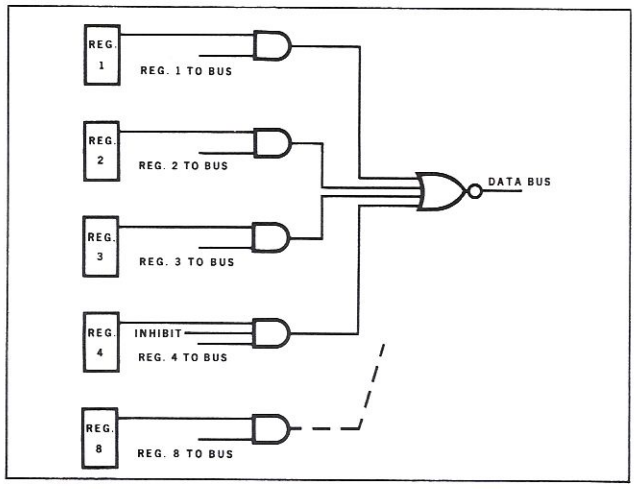

Fig. 3. Register to bus gating.

BINARY COMPARATOR

The 9008 can be used in conjunction with NAND gates to build binary comparators. A two-bit comparator is shown in Fig. 4. The expander inputs can be used for additional capability and for large word lengths the outputs of several 9008 elements can be fed into a NAND gate to produce the equivalence function. A design of a 32-bit comparator using 9008, 9007, and 9002 TTμL circuits has a typical delay of 30 nanoseconds.

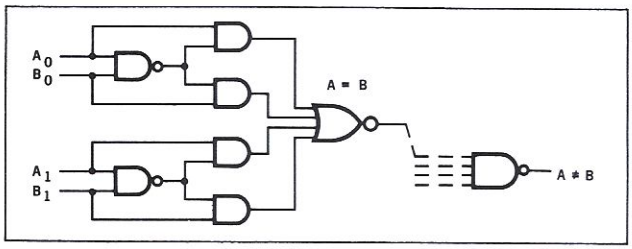

Fig. 4. Two-bit comparator.

ADDERS

Two 9008's will form a full carry-dependent-sum adder as shown in Fig. 5 below.

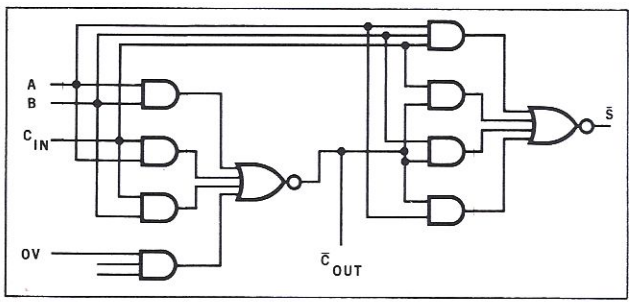

Fig. 5. Carry dependent sum adder.

The Boolean functions generated by 9008 elements connected in this manner are

$$\overline{C_{out}} = \overline{AB + BC_{IN} + C_{IN}A}$$

$$\bar{S} = A \oplus B \oplus \bar{C}_{IN} = A \oplus \bar{B} \oplus C_{IN} = \bar{A} \oplus B \oplus C_{IN}$$

If two 9008 elements are connected in the above manner and the resulting functional block represented in Fig. 6, the following designs will be simplified.

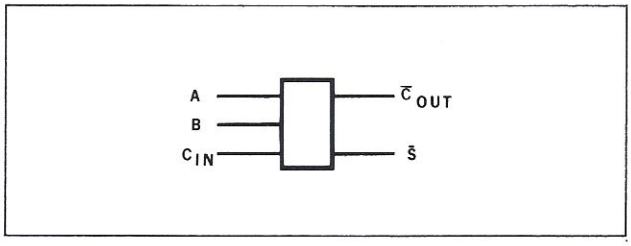

Fig. 6. Functional block of two 9008's connected as an adder.

With inverted inputs, the building block produces the assertion sum and carry (Fig. 7).

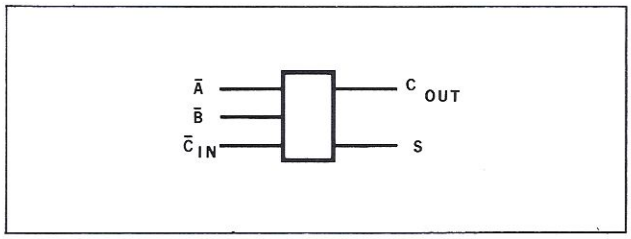

Fig. 7. Functional block with negated inputs.

It can be seen from Fig. 8 that a number of these building blocks can be connected together to form a high-speed ripple-through parallel adder, where the carry delay is only one AND-NOR gate per stage. Inverters can be placed at the A and B inputs of every other stage and also at the sum output of the remaining stages, so that assertion inputs are required and assertion sum outputs result. The delay to the final sum is (N + 1) AND-NOR gates, where N is the number of adder stages.

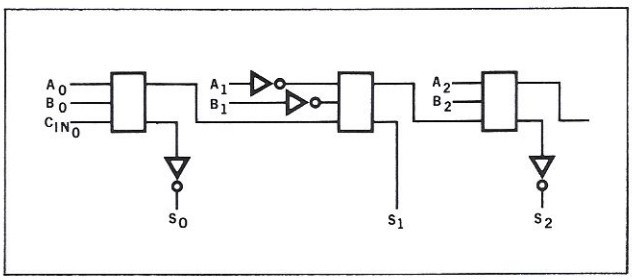

Fig. 8. Ripple - through parallel adder.

In a practical system the inverters can often be omitted, since the inputs can be obtained from either the assertion or negation outputs of register stages, and either the assertion or the negation signal can be used to write into a register stage.

The building block formed from two 9008's can be used to build carry-save adders for high-speed multiplication and division. Any number of variables can be added using the building block. A typical example for adding six variables is shown in Fig. 9.

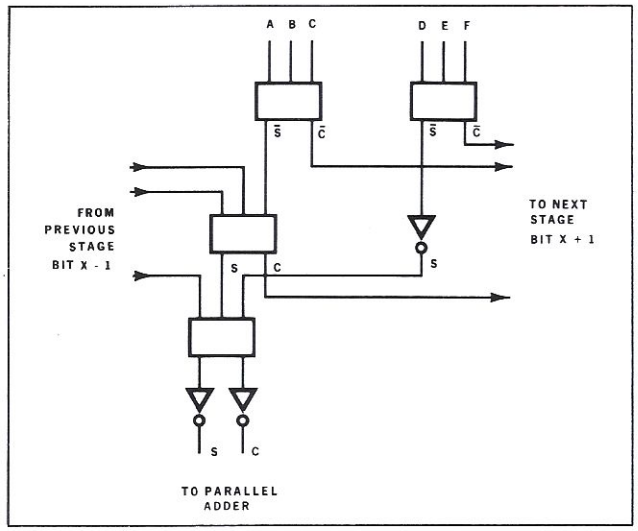

Fig. 9. Addition of six variables.

The delay from the input to the output to the parallel adder is seven AND-NOR gates or about 70 nanoseconds, which allows an extremely high-speed multiplication to be performed.

PARITY CHECKING

Since we have the function $F = A \oplus B \oplus \overline{C}$ formed by two elements, the parity function can be easily generated. Four of the building blocks can be used to form a nine-bit parity checker or generator. An example is shown in Fig. 10 for a nine-bit odd parity generator.

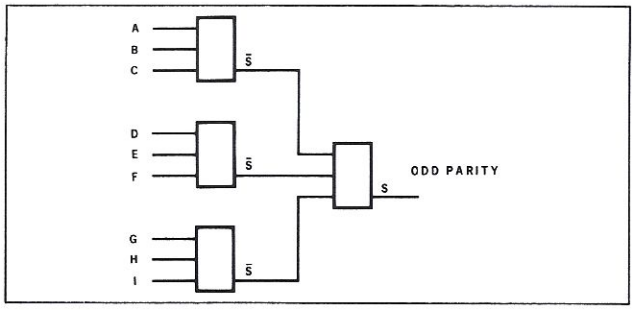

Fig. 10. Nine-bit parity generator.

The method is not limited to nine bits, but can be extended to any number of bits using additional blocks. The above design produces the outputs with a delay of four AND-NOR gates; about 40 nanoseconds.

SEQUENTIAL CIRCUITS

The 9008 can be used as a latch with the addition of an inverter (see Fig. 11) . Only three of the four available AND gates are required, the fourth AND gate can conveniently be used for presetting the latch.

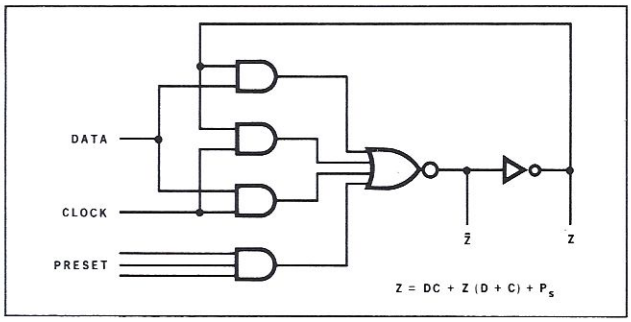

Fig. 11. The 9008 used as a latch.

Using the above latch as a building block, various counters can be designed. An example of a counter designed around this latch with its associated timing diagram is shown in Fig. 12.

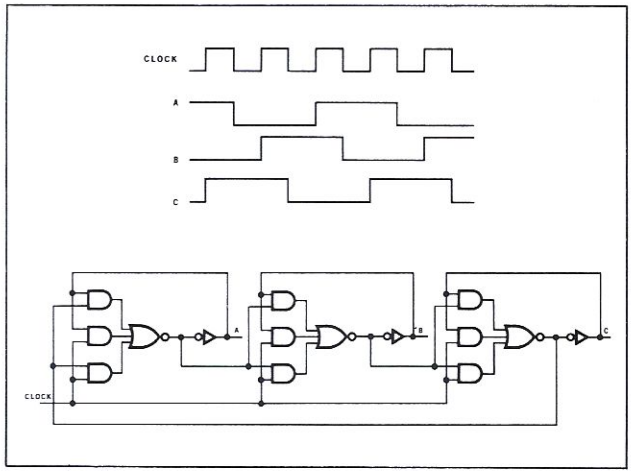

Fig. 12. Example of typical counter using 9008.

SUMMARY

The 9008 TTμL AND-NOR element can be used for a multitude of tasks other than those described above. The logical designs shown only indicate the capability of the device.

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